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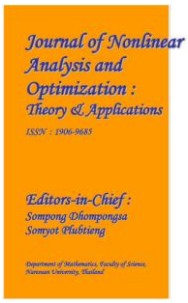

IMPROVED DESIGN OF CMOS 1-BIT COMPARATOR WITH STACKING TECHNIQUE

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ABSTRACT The comparator is an electronic circuit which compares the magnitude of one signal to another signal. The comparators are used in analog to digital converters. Comparator is the "Heart" of the Analog to digital converter (ADC). As we talk about the VLSI technology, in this environment the device should be of higher speed, less cost and low power consumption. Many of the electronic devices like mobile devices and other portable computing devices have constraints in terms of power consumption. Power consumption is one of the important factors of VLSI circuit design for CMOS is the primary technology. The power consumption has become a fundamental problem in VLSI circuit design. Therefore, reducing the power consumption of integrated circuits through design improvement is a major challenge in portable system design. To solve the power consumption problem, many different techniques from circuit level to device level and above have been proposed by researchers. This paper presents the design and analysis of a CMOS based efficient one bit comparator circuit. Comparator has been designed and simulated in 180nm TSMC technology. The proposed circuit uses a XNOR gate, two AND gates and two NOT gates. Stacking technique has been used to improve the conventional design. Power supply has been varied from 1.0V to 2.8V for the proposed and basic design. Result reflects that proposed approach shows less power consumption and improved power delay product (PDP).

I. INTRODUCTION TO VLSI

VLSI TECHNOLOGY VLSI

Design presents state-of-the-art papers in VLSI design, computer-aided design, design analysis, design implementation, simulation and testing. Its scope also includes papers that address technical trends, pressing issues, and educational aspects in VLSI Design. The Journal provides a dynamic high-quality international forum for original papers and tutorials by academic, industrial, and other scholarly contributors in VLSI Design.

The development of microelectronics spans time which is even lesser than the average life expectancy of a human, and yet it has seen as many as four generations. Early 60's saw the low density fabrication processes classified under Small Scale Integration (SSI) in which transistor count was limited to about 10. This rapidly gave way to Medium Scale Integration in the late 60's when around 100 transistors could be placed on a single chip.

It was the time when the cost of research began to decline and private firms started entering the competition in contrast to the earlier years where the main burden was borne by the military. Transistor-Transistor logic (TTL) offering higher integration densities outlasted other IC families like ECL and became the basis of the first integrated circuit revolution. It was the production of this family that gave impetus to semiconductor giants like Texas Instruments, Fairchild and National Semiconductors. Early seventies marked the

growth of transistor count to about 1000 per chip called the Large Scale Integration.

By mid-eighties, the transistor count on a single chip had already exceeded 1000 and hence came the age of Very Large Scale Integration or VLSI. Though many improvements have been made and the transistor count is still rising, further names of generations like ULSI are generally avoided. It was during this time when TTL lost the battle to MOS family owing to the same problems that had pushed vacuum tubes into negligence, power dissipation and the limit it imposed on the number of gates that could be placed on a single die The second age of Integrated Circuits revolution started with the introduction of the first microprocessor, the 4004 by Intel in 1972 and the 8080 in 1974. Today many companies like Texas Instruments, Infineon, Alliance Semiconductors, Cadence, Synopsys, Celox Networks, Cisco, Micron Tech, National Semiconductors, ST Microelectronics, Qualcomm, Lucent, Mentor Graphics, Analog Devices, Intel, Philips, Motorola and many other firms have been established and are dedicated to the various fields in "VLSI" like Programmable Logic Devices, Hardware Descriptive Languages, Design tools, Embedded Systems etc.

In 1980s, hold-over from outdated taxonomy for integration levels. Obviously, influenced from frequency bands, i.e., HF, VHF, and UHF. Sources disagree on what is measured (gates or transistors)

SSI – Small-Scale Integration (0-102)

MSI – Medium-Scale Integration (102 -103)

LSI – Large-Scale Integration (103 -105)

VLSI – Very Large-Scale Integration (105 - 107)

ULSI – Ultra Large-Scale Integration (>= 107)

VLSI Technology, Inc. was a company which designed and manufactured custom and semi-custom ICs. The company was based in Silicon Valley, with headquarters at 1109 McKay Drive in San Jose, California. Along with LSI Logic, VLSI Technology defined the leading edge of the application-specific integrated circuit (ASIC) business, which accelerated the push of powerful embedded systems into affordable products. The company was founded in 1979 by a trio from Fairchild Semiconductor by way of Synertek - Jack Balletto, Dan Floyd, and Gunnar Wetlesen - and by Doug Fairbairn of Xerox PARC and Lambda (later VLSI Design) magazine.

II. LITERATURE SURVEY:

"Design Analysis of 1-bit CMOS comparator"

This paper presents a comprehensive overview of CMOS digital integrated circuit design, emphasizing analysis and optimization techniques for low power consumption. CMOS technology, which leverages complementary and symmetrical pairs of p-type and n-type MOSFETs, is the foundation of modern digital circuits due to its inherent low power dissipation characteristics. The primary components of power consumption in CMOS circuits, dynamic and static power, are analyzed, with dynamic power arising from charging and discharging load capacitances during transistor switching, and static power resulting from leakage currents in inactive transistors.

Key optimization techniques for reducing power consumption are discussed, including voltage scaling, threshold voltage adjustment, clock gating, power gating, and various architectural and algorithmic strategies. Voltage scaling, particularly dynamic voltage and frequency scaling (DVFS), significantly reduces power by adjusting voltage and frequency according to workload demands. Threshold voltage adjustments, through multi-threshold CMOS (MTCMOS), balance speed and leakage power by employing transistors with varying threshold voltages.

Clock gating minimizes unnecessary switching activity by disabling the clock signal to idle circuit portions, while power

gating reduces leakage power by disconnecting the power supply to inactive blocks using sleep transistors. Architectural optimizations, such as parallelism and pipelining, distribute workload across multiple processing units and pipeline stages, reducing peak power demands. Additionally, data encoding techniques and logic style optimizations further enhance power efficiency.

The paper also highlights core components in low-power CMOS VLSI design, including standard cells, memory blocks, power management units, clock distribution networks, and low-power I/O circuits. Through these techniques and design considerations, the paper aims to provide a detailed framework for designing energy-efficient CMOS digital integrated circuits, crucial for the development of portable and battery-operated devices.

The increasing demand for portable and battery-operated electronic devices has intensified the focus on minimizing power consumption in CMOS circuits. A significant portion of this power consumption is attributed to leakage currents, which persist even when transistors are in the off state. This paper explores advanced models and algorithms aimed at accurately estimating and effectively bounding leakage power in CMOS circuits.

We present a detailed analysis of various leakage mechanisms, including subthreshold leakage, gate oxide leakage, and junction leakage, each contributing to the overall static power dissipation. Our approach begins with the development of precise leakage models that account for process variations, temperature effects, and supply voltage scaling. These models serve as the foundation for the subsequent algorithmic techniques designed to estimate and bound leakage power.

"Models and Algorithms for Bounds on Leakage in CMOS Circuits,"

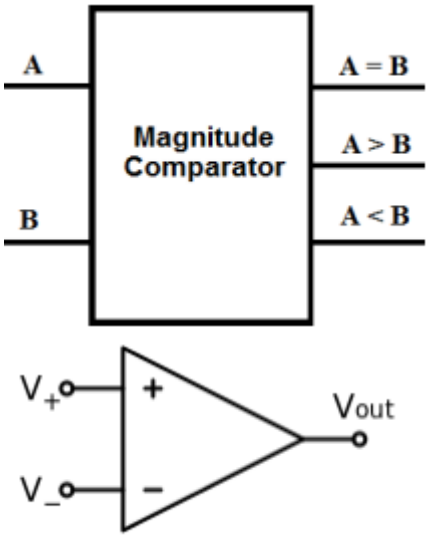
The proposed algorithms leverage a combination of analytical methods and heuristic strategies to achieve optimal trade-offs between accuracy and computational efficiency. Key techniques include statistical modeling of process variations, optimization of transistor sizing, and the implementation of multi-threshold CMOS (MTCMOS) strategies to selectively apply high-threshold transistors in non-critical paths.

Additionally, we explore power gating techniques, which involve the use of sleep transistors to disconnect the power supply from inactive circuit blocks, effectively reducing leakage during idle periods. Our algorithms also incorporate dynamic threshold voltage scaling (DVTS) and adaptive body biasing to further minimize leakage in active regions of the circuit.

Through comprehensive simulations and experimental results, we demonstrate the effectiveness of our models and algorithms in achieving significant reductions in leakage power. The methodologies presented in this paper provide a robust framework for designers seeking to develop low-leakage CMOS circuits, thereby enhancing the energy efficiency and battery life of modern electronic devices.

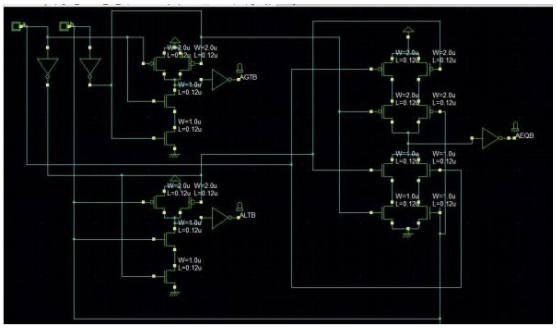
III.EXISTING ARCHITECTURE:

EXISTING COMPARATOR: The comparator is basically 1-bit analog to digital converter. Fig.3.1 shows general block diagram of comparator and Fig.3.2 shows symbol of comparator.



Input		Output		
A	B	YA=B	YA>B	YA<B
0	0	1	0	0
0	1	0	0	1
1	1	0	1	0
1	1	1	0	0

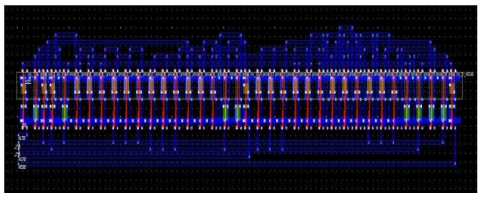
The equation for A=B is AΘB (1) The equation for A>B is A (2) The equation for A



Existing comparator circuit diagarm

The basic 1 bit Comparator circuit consist of three basic building blocks, two AND gates and one XNOR gate. Each AND gate consists ofsix MOSFET, three PMOS and three NMOS. XNOR gate consists of fourteen MOSFET, seven PMOS and seven NMOS. The comparator basically a analog to digital converter, Analog signal is converted into digital signal with the help of sampling. The sampling frequency (fs) is defined as the reciprocal of time period T. A comparator circuit compares two voltages and outputs either a 1 (the voltage at the plus side; VDD in the illustration) or a 0 (the voltage at the negative side) to indicate which is larger. Comparators are often used, for example, to check whether an input has reached some predetermined value. In most cases a comparator is implemented using a dedicated comparator IC, but op-amps may be used as an alternative. In practice, this circuit can be improved by incorporating a hysteresis voltage range to reduce its sensitivity to noise.

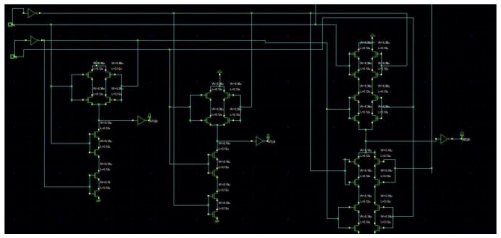
LAYOUT DIAGRAM:



It has two inputs, inverting and non-inverting and an output . But it is specifically designed to compare the voltages between its two inputs. Therefore it operates in a non-linear fashion. The comparator operates open-loop, providing a two-state logic output voltage. Comparators can give precision measurements, with consistent accuracy by eliminating human error. They are employed to find out, by how much the dimensions of the given component differ from that of a known datum.

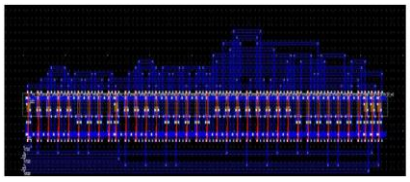
IV.PROPOSED ARCHITECTURE:

PROPOSED COMPARATOR : In this work the stacking techniques has been applied to conventional comparator to reduce the power consumption. In stacking technique every transistor is divided into two transistors each have W/L is half of parent transistor as shown in the Fig.4. The number of transistor increases but area is not affected much since W of parent transistor is divide into two transistor of W/2 width each.



When two transistors are turned off together induced reverse bias between the two transistors results decrease in power. This technique is based on the fact that natural stacking of MOSFET helps in achieving leakage current. The leakage through two series OFF transistor is much lower than that ofsingle transistor because ofstack effect . An effective way to reduce leakage power in active mode is stacking of transistor . In proposed comparator circuit there are three building blocks, two AND gates and one XNOR gate. Each AND gate consists ten MOSFETS, five PMOS and five NMOS each. XNOR gate consist of twenty two MOSFETS including eleven NMOS and eleven PMOS. The proposed comparator circuit is shown in Fig.6. For AGTB and ALTB, AND 19 gate has been used because in AND gate whenever both inputs are high then output will be high otherwise output will be zero. For AETB a XNOR gate has been used as in XNOR gate whenever both inputs are same then output will be high otherwise it will be zero. The basic comparator circuit shown in Fig.5 and proposed comparator circuit shown in Fig.6 In n Bit comparator the truth table consists 22n terms in which number of terms for equal condition will be 2n and for greater than and less than number of terms will be In 1 bit comparator number of AETB conditions are 2 and number of AGTB or ALTB conditions.

LAYOUT DIAGRAM:



Results of proposed and conventional comparator has been obtained in TSMC 180nm technology for different power supply voltages varying from 1.0 V to 2.8V. The simulation waveform of 1- bit conventional comparator.

V.ADVANTAGES & APPLICATIONS

ADVANTAGES

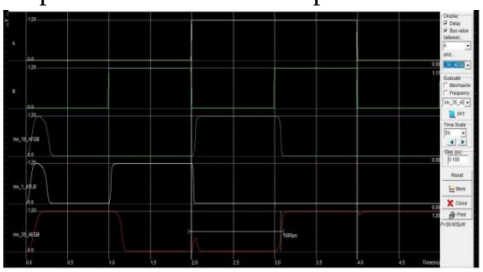
1. Power consumption decreases
2. leakage power decreases
3. It improves model performance
4. It can reduce bias
5. High degree of reliability
6. Used to predict multiple nodes
7. It helps to automatically clean up the objects.

APPLICATIONS

1. Laboratory standards
2. Working gauges
3. Analog conversion
4. Over-limit alarms
5. It can be used for backtracking
6. Signal applications
7. Used for systematic memory management

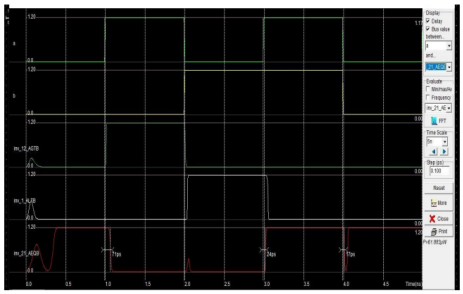
VI.RESULT:

Proposed Architecture Output waveforms:



Power = 39.00x10-6watts

Existing Architecture Output Waveforms:



Power = 61.88x10-6watts

Approach type	Power(pWatt)	Delay(nS)	PDP (atto Joule)
Basic Comparator	61.88	49.67	14.3
Proposed Comparator	39.00	49.38	8.6

VII.CONCLUSION:

In this work a new design of comparator has been proposed and power consumption, delay and PDP results have been obtained for the basic design and proposed circuit. The Proposed Comparator has less power consumption, less delay and less PDP as compared to basic comparator. It is noticed that the power consumption in proposed

comparator is 174.352pWatt whereas the power consumption in basic comparator circuit is 287.93 pW, in terms of delay the delay in both circuits are almost same there is very little difference, PDP of proposed comparator is smaller than basic comparator. Proposed comparator shows less power consumption and improved power delay product.

FUTURE SCOPE:

We can extend this design to 'n'bit comparator and we apply these designs to any application in future a single circuit can be designed such that the circuit can be programmed for any type of biosignal sensing. Moreover, ECG signal sensing circuit can be designed with the help of on-chip peripherals present on the FPGA board. Further with rapid increase in the technology, a new technological solutions and new architectures can be developed to meet the need of technology scaling. In addition, with continuous improvement in CMOS technology, researchers can focus on CMOS IC design techniques for wireless medical and health care applications with a high level of integration and low power consumption. Across the basis of new technology, there is room to develop construction strategies at both the circuit block level and the system level. CMOS IC design strategies for the whole signal chain of wireless medical and health care networks deployed at low-technological nodes, with focus on ultra-low-power IC design techniques

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